CLAIMS

1. A model for representing a bidirectional wire input/output (I/O) during computer simulation of a electronic device, the model comprising:

a) a first path between a first port and a second port;

b) a second path between the second port and the first port; and

c) a control mechanism, the control mechanism checking signal values on the first port and the second port when a change is detected on the first port or the second port, the control mechanism enabling the first path when a change is detected on the first port and the first port does not equal the second port, the control mechanism enabling the second path when a change is detected on the second port and the first port does not equal the second port.

2. The model of claim 1 wherein the model is implemented in the Verilog hardware description language.

3. The model of claim 1 wherein the model is implemented in the VHDL hardware description language using Vital timing routines.

4. The model of claim 1 wherein the first path comprises a second NMOS device and a fourth NMOS device, and wherein the second path comprises a first NMOS device and a third NMOS device.

5. The model of claim 4 wherein the control mechanism enables the first path by enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism enables the second path by enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port.

6. The model of claim 4 wherein the first NMOS device, the second NMOS device, the third NMOS device, and the fourth NMOS device comprise Verilog NMOS primitives.

7. The model of claim 4 wherein timing values are annotated in the model and include module input port delays annotated into the third NMOS device and the fourth NMOS device.

8. The model of claim 1 wherein timing values are annotated across the first path and the second path.

9. The model of claim 8 wherein the timing values are annotated in the form of propagation delays annotated between the first port to the second port and between the second port to the first port.

10. The model of claim 1 wherein the control mechanism further disables the second path when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism further disables the first path when a change is detected on the second port and the first port does not equal the second port.

11. A model for representing a bidirectional wire input/output (I/O) during computer simulation of a electronic device, the model comprising:

a) a first path between a first port and a second port, the first path including a second NMOS device,

b) a second path between the second port and the first port, the second path including a first NMOS device; and

c) a control mechanism, the control mechanism checking signal values on the first port and the second port when a change is detected on the first port or the second port, the control mechanism enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, the control mechanism enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port.

12. The model of claim 11 wherein the second path further includes a third NMOS device and wherein the first path further includes a fourth NMOS device, wherein the third and fourth NMOS devices are tied on to function as pass devices.

13. The model of claim 12 wherein the timing values are annotated into the model in the form of module input port delays annotated into the third NMOS device and the fourth NMOS device.

14. The model of claim 11 wherein the timing values are annotated into the model in the form of propagation delays across the first path and the second path.

15. The model of claim 11 wherein the first and second NMOS devices comprise Verilog NMOS primitives.

16. The model of claim 11 wherein the control mechanism further disables the first NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism further disables second NMOS device when a change is detected on the second port and the first port does not equal the second port.

17. A method for representing a bidirectional wire input/output (I/O) during computer simulation of an electronic device, the method comprising:

a) providing a model for the bidirectional wire I/O, the model including:

i) a first path between a first port and a second port; and

ii) a second path between the second port and the first port;

b) checking signal values on the first port and the second port when a change is detected on the first port or the second port;

c) enabling the first path when a change is detected on the first port and the first port does not equal the second port;

d) enabling the second path when a change is detected on the second port and the first port does not equal the second port.

18. The method of claim 17 further comprising the steps of:

e) disabling the second path when a change is detected on the first port and the first port does not equal the second port;

f) disabling the first path when a change is detected on the second port and the first port does not equal the second port.

19. The method of claim 17 further comprising the step of annotating timing values across the first path and the second path.

20. The method of claim 17 wherein the model further includes a wherein a second NMOS device and a fourth NMOS device in the first path and further includes a first NMOS device and a third NMOS device in the second path.

21. The method of claim 20 further comprising the step of annotating module input port delays into the third NMOS device and the fourth NMOS device.

22. A program product comprising:

A) a hardware description language model for representing a bidirectional wire input/output (I/O) during computer simulation of a electronic device, the hardware description language model including:

i) a first path between a first port and a second port;

ii) a second path between the second port and the first port; and

iii) a control mechanism, the control mechanism checking signal values on the first port and the second port when a change is detected on the first port or the second port, the control mechanism enabling the first path when a change is detected on the first port and the first port does not equal the second port, the control mechanism enabling the second path when a change is detected on the second port and the first port does not equal the second port;

B) signal bearing media bearing the hardware description language model.

23. The program product of 22 wherein the signal bearing media comprises transmission media.

24. The program product of 22 wherein the signal bearing media comprises recordable media.

25. The program product of claim 22 wherein the model is implemented in the Verilog hardware description language.

26. The program product of claim 22 wherein the model is implemented in the VHDL hardware description language using Vital timing routines.

27. The program product of claim 22 wherein the first path comprises a second NMOS device and a fourth NMOS device, and wherein the second path comprises a first NMOS device and a third NMOS device.

28. The program product of claim 27 wherein the control mechanism enables the first path by enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism enables the second path by enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port.

29. The program product of claim 27 wherein the first NMOS device, the second NMOS device, the third NMOS device, and the fourth NMOS device comprise Verilog NMOS primitives.

30. The program product of claim 27 wherein timing values are annotated into the model that include module input port delays annotated into the third NMOS device and the fourth NMOS device.

31. The program product of claim 22 wherein timing values are annotated across the first path and the second path.

32. The program product of claim 31 wherein the timing values are annotated in the form of propagation delays annotated between the first port to the second port and between the second port to the first port.

33. The program product of claim 22 wherein the control mechanism further disables the second path when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism further disables the first path when a change is detected on the second port and the first port does not equal the second port.

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